Section I. Amendments to the Claims

Please amend claims 40, 47, 49, 51, 61 and 63, and add new claim 64, as set out below in the listing of claims 1-64 of the application.

1-39. (Cancelled)

40. (Currently Amended) A microelectronic device structure comprising:

a silicon substrate comprising at least one additional layer selected from the group consisting of a bottom electrode layer, a diffusion barrier layer, an insulating layer and a buffer layer;

a ferroelectric oxide film material positioned over the silicon substrate, wherein the ferroelectric oxide material has a top surface and vicinity thereunder that is substantially stoichiometrically complete in oxygen concentration;

a top electrode comprising a ~~first layer~~ top surface and a bottom surface ~~second layer~~, wherein the bottom surface ~~first layer~~ directly contacts the top surface of the ferroelectric oxide film material and ~~the second layer directly contacts the first layer, wherein the first layer of the top electrode~~ comprises a metal oxide material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof, and the top surface ~~second layer~~ of the top electrode consists of a metal ~~is~~ selected from the group consisting of Ir, Rh and mixtures thereof, ~~and wherein the total thickness of the top electrode is in a range from about 100 nm to about 500 nm~~ wherein the transition from the bottom surface of the top electrode to the top surface of the top electrode is increasingly metallic.

41. (Previously Presented) The microelectronic device structure according to claim 40, wherein said ferroelectric film comprises an oxide perovskite or layered structure perovskite.

42. (Previously Presented) The microelectronic device structure according to claim 40, wherein said ferroelectric film comprises a material selected from the group consisting of

lead zirconium titanate, barium and/or strontium titanates, and strontium bismuth tantalates.

43. (Previously Presented) The microelectronic device structure according to claim 40, wherein said ferroelectric film comprises a lead zirconium titanate material.

44. (Previously Presented) The microelectronic device structure according to claim 40, wherein said ferroelectric film comprises a barium and/or strontium titanate material.

45. (Previously Presented) The microelectronic device structure according to claim 40, wherein said ferroelectric film comprises a strontium bismuth tantalate material.

46. (Cancelled)

47. (Currently Amended) The microelectronic device structure according to claim 40, wherein said ~~first layer of the~~ top electrode comprises ~~is formed of~~ an Ir oxide material.

48. (Cancelled)

49. (Currently Amended) The microelectronic device structure according to claim 40, wherein said ~~second layer of the~~ top electrode comprises ~~is formed of~~ Ir.

50. (Cancelled)

51. (Currently Amended) The microelectronic device structure according to claim 40, wherein the top electrode comprises an Ir oxide material and Ir ~~is formed of a first layer of IrO_2 and a second layer of Ir~~.

52. (Cancelled)

53. (Cancelled)

54. (Cancelled)

55-60. (Cancelled)

61. (Currently Amended) The microelectronic device structure according to claim 40, wherein said ~~second layer of the~~ top electrode comprises ~~is formed of~~ Rh.

62. (Cancelled)

63. (Currently Amended) A ferroelectric or high ε capacitor comprising:

a silicon substrate comprising at least one additional layer selected from the group consisting of a bottom electrode layer, a diffusion barrier layer, an insulating layer and a buffer layer;

a thin film of an ferroelectric oxide material positioned over the bottom electrode, wherein the thin film of ferroelectric oxide material has a top surface that is substantially stoichiometrically complete in oxygen concentration, wherein said ferroelectric oxide material comprises a material selected from the group consisting of lead zirconium titanate, barium and/or strontium titanates, and strontium bismuth tantalates; and

a top electrode comprising a top surface ~~first layer~~ and a bottom surface ~~second layer~~, wherein the bottom surface ~~first layer~~ directly contacts the top surface of the thin film of ferroelectric oxide material and ~~the second layer directly contacts the first layer, wherein the first layer is formed~~ consists essentially of a metal oxide material selected from the group consisting of Ir oxides, Rh oxides, and mixtures thereof, and the top layer ~~second layer~~ consists essentially of a metal ~~is~~ selected from the group consisting of Ir, Rh and mixtures thereof~~, wherein the total thickness of the top electrode is in a range from about 100 nm to about 500 nm~~, wherein the transition from the bottom surface of the top electrode to the top surface of the top electrode is increasingly metallic, and wherein the oxygen concentration of the ferroelectric oxide film is maintained during the formation of the bottom surface of the top electrode without the need for post-deposition annealing in oxygen.

64. (New) The microelectronic device structure according to claim 40, wherein said top electrode comprises an Rh oxide material.